Amendments to the Specification

Please replace the paragraph that was inserted before the first line of the specification with the following amended version of that paragraph:

This application is a continuation of copending, commonly assigned United States Patent Application No. 09/775,597, filed February 5, 2001, now U.S. Patent No. 6,682,981, which is a continuation of United States Patent Application No. 09/027,959, filed February 23, 1998, now abandoned, which is a division of United States Patent Application No. 08/850,749, filed May 2, 1997, now U.S. Patent No. 5,985,693, which is a continuation of United States Patent Application No. 08/315,905, filed September 30, 1994, now U.S. Patent No. 5,869,354, which is a division of United States Patent Application No. 07/865,412, filed April 8, 1992, now U.S. Patent No. 5,354,695, all of which are incorporated by reference herein in their entireties.

Please replace the paragraph at page 24, lines 10-34 with the following amended version of that paragraph:

The Air Tunnel structure in one embodiment is fabricated with CVD processing techniques; alternatively, ECR (Electron-Cyclotron-Resonance) plasma CVD processing may soon provide an alternative deposition method. The gaseous dielectric separation of a conductor or a semiconductor device is accomplished by forming a sacrificial CVD film of a-Si, polysilicon or alternate material (typically dielectric material) that can be deposited by CVD means and selectively etched versus the other MDI circuit membrane material layers.

Anticipating the use of Air Tunnel interconnect structures in the fabrication of a circuit membrane, semiconductor devices are isolated ~~(passivated)~~ by trench isolation of each device, and depositing a thin layer of oxide or nitride (typically less than 2,000 Å thick) over exposed device surfaces, and then depositing a film of a-Si. The thickness of the a-Si film and the width of the isolation trench are chosen such that the trench is plugged or filled evenly leaving the surface over the plug relatively planar. This plug technique is facilitated by CVD process technology which deposits films conformally on all interacting surfaces. Subsequent Air Tunnel interconnect structures are completed and the a-Si layers are removed by a silicon selective etchant; the etchant accesses the a-Si through the etch-vias as explained below.